The TMS32010. The DSP chip that changed the destiny of a semiconductor giant.

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As co-founders of the TMS 32010 DSP group, many of us worked in a closely knit team, in a warehouse like building, with one desire - produce a commercially successful DSP chip. We were fortunate enough to realize the dream with a combination of technical innovation of team members, TI management support and TI's technology prowess. Most engineers start out with such a dream but only a few are lucky enough to get an ideal opportunity to realize it. Well, we were lucky . We believed enough to work hard and had a feeling that we were on to something big. But yes, we never could have imagined that our pioneering DSP work will one day change the course of entire TI.

(Surrendar Magar 23rd Oct 1998).

Abstract.

This is the history of the design program for the first Digital signal processor chip in Texas Instrument's TMS 320 family written from the background leading up to the formation of the design team and concentrating on the people behind the chip and how it came into being.

Over the years many people have contributed to the success of TI's Digital Signal Processing strategy. Some are still with TI but many others have moved on into new careers in other companies. It seems fitting on this 25th anniversary of the first functional chip to share the history of the design program and acquaint those Tiers, who have since joined the TI family, how a few engineers were lucky enough to see their efforts write the course of history and lay the first stepping stone for TI to become the world leader in Digital Signal Processing.

The Early Days

The major emphasis in Microprocessor activity in TI in the mid to late 70's was promoting the 9900 strategy. Back then TI had a management committee composed of a group of VP's and in 1978 the committee decided that TI was not making the needed headway in the uP (Microprocessor) market (used then to include uC's (Micropcomputers) and that SC needed an infusion of people with a systems background from other parts of TI. They recruited Wally Rhines,(now CEO of Mentor Graphics) John Hughes, Ken Wickham, Kurt Beohnke and Jim Carlo specifically to do this. The MMP (Microprocessor, Microcomputer Products) division resulted from this infusion of people and was headed up by Wally Rhines in a separate building located at Commerce Park in Houston.

In those days ,TI held once a year week long meetings where each TI business defined the outline of its strategy for the future. Harvey Cragon's presentation suggested a Digital Signal Processor oriented device and John Hughes followed up with Harvey and suggested that a group be formed of people from around TI to develop an architecture specification for a DSP. The idea received the interest of Bill Holton, Manager SREL (Semiconductor Research Engineering Lab), and in charge of the purse strings for TI OST (Objectives, Strategy and Tactics) development programs, and Harvey's supervisor at the time. He instructed Harvey to set up a study group to develop the architecture. Harvey's study Group was led by himself, with initial members Stu Barab,Charles Buenzli, Ed Caudel, Mickey Dewitt, Ed Hassler, Dale Ezell, Glen Haas, Mark Pavicic and Tim Smith. A number of working meetings were held in 1979 culminating in a Digital Signal Microcomputer architecture specification and called the SPC (Signal Processing Computerr). Harvey Cragon's article published in the 1996 issue of the TI technical journal provides more insight into the events leading up to the release of an initial architecture spec from the work of this study group and compiled by Ed Caudel.

At this time the SPC activity had not surfaced as a major interest in the TI reporting structure. MMP was mainly concerned with promoting the 9900 strategy most of which were Microcontrollers (Microcomputers) since they only had on chip memory or limited memory reach and mostly on chip peripherals using the CRU (Communication Register Unit) for external I/O. The 9900 was the only true Micro-processor (uP).

The Ashtray Incident (ATI)

This story is a classic in the annals of TI history and it is worth including since it does play a part in the history of the DSP in TI. This is Wally Rhines and John Hughes account of the famous ashtray incident that became known as the ATI. In early 1980 Wally Rhines was giving a presentation to Fred Bucy (TI's CEO at the time) and John Hughes was flipping the foils. The meeting had been called by DSG (Data systems group) who needed a follow up device to the 9900 for their 990 minicomputers and Wally was presenting the MMP strategy. The Microprocessor strategy team knew they had to do this given Fred et al's strategic interest in the

computer business so they attempted to craft a modest risk approach that would satisfy DSG's needs and give TI one last shot at trying to penetrate the uP market for SC. Security analysts had been telling Fred daily that Motorola and Intel were going to take over the semiconductor industry with their host microprocessors and Fred wanted an answer that would put TI back in the ball game. John recalls that they had some DSG performance benchmarks that could be met using 5um NMOS technology and thus avoiding what had been judged to be a higher risk 2.5um technology. DSP was not on the radar screen at all yet – at least with Bucy et al. Bottom line was that Wally proposed meeting the DSG need with a conservative 5um NMOS 99000 design. Unfortunately Wally had not been present for an earlier glowing presentation by Larry Wall on all the good things that HPD (Houston Process Development) were doing with 2.5um NMOS. MOS Memory group were already developing the 2147 fast 4K SRAM (Static Random Access Memory) in 2.5um NMOS. Fred had been well primed for the following reaction. With the proposal that MMP was going to be conservative and do the 99000 in 5um NMOS Fred blew up. Shouting, "If you cant do it I'll find someone who can" , he threw a large glass ashtray at Wally. Fortunately no damage was done other than to the ashtray and MMP came away knowing what the priorities were in relation to process development for the 99000 and also for the SPC.

The Architecture

In 1978 Ed Caudel worked in the MMP design department reporting to the design manager Jerry Rogers. As already mentioned the thrust of TI's MMP group was in promoting the TMS 9900 family. Ed Caudel was working on the redesign of the TMS 9940 micro controller and had expressed an interest in working on the SPC. Since Ed and Jerry did not see eye to eye on many issues, Ed was reassigned to the systems group reporting to John Hughes. Ed was the first person to be fully employed on the SPC and developed the initial architecture spec for the development of the SPC in conjunction with Harvey and the other members of the work study group.

It was just before the 1979 ISSCC conference that John Hughes became aware of a paper to be presented by Intel on a Digital Signal Processing integrated circuit the i2920. The paper caused a lot of excitement in TI both in MMP and TI management. The concern was that Intel had beat TI again. It purported to be the next greatest thing and top TI management was concerned how TI could respond. The SPC was the answer but this was not sufficient to satisfy their concerns. The i2920 paper was forwarded around TI where it was ultimately concluded that the device did not have enough bits of resolution with its on chip A/D and D/A, caused application and production risk and that the 2920 lacked a hardware on chip multiplier. The publication of the Intel paper was the event that moved the SPC out of the shadows and into the lime light. Intel's paper had done more to convince management that MMP was on the right track than the technical work up to that point.

Intel certainly had pipped TI to the post with the i2920 as far as DSP was concerned. Fortunately for TI they chose not to pursue their lead which left the field open for TI. Today, 25 years later they are trying to play catch up.

The Design Team

At the same time as the previous events were unfolding in 1978/79, Tony Leigh was working in the TI UK Bedford design center on a VMOS memory mapper chip design as a peripheral to support the 9900 strategy. He had just returned from an ex-pat assignment in the US where he was the design manager for TI's 4 K static ram program- the TMS 4044/4045. The memory mapper was a fall out from the MOS memory initiative to promote AMI's VMOS technology which was the brain child of T.J.Rogers (Now CEO of Cyprus semiconductors). The MOS memory design department under Dick Gossen had embarked on a dual program to investigate a 2.5um NMOS process (SMOS) and a 1um VMOS process for the purpose of marketing a fast 4K static to compete with Intel's 2147. Cliff Rhodes headed the SMOS version and Dan Kang headed the VMOS version both reporting to Bill Bruncke. In a decision forced by Don Brooks at an OST (Objective, Strategies & Tactics) review in Jan 1979 the complexity of VMOS lost out to the simplicity of SMOS in the decision for the process for the fast 4K static. This all but left VMOS dead in the water but Wally Rhines resurrected it in a deal to second source AMI's VMOS process in exchange for AMI to second source TI's 9900 family. Non of this eventually came to fruition.

Start of the 320 Design Program

In the summer of 1979 Tony traveled to TI in Houston and AMI in San Jose for a design review of the memory mapper. It was during this visit to Houston that Jerry Rogers sounded Tony out for the position of Design Manager for the SPC. He formally accepted the position on his return to England after working with Ed Caudel on the current status of the architecture spec. A date was negotiated for him to leave TI UK in January of 1980 after completing work on the TMS 9995 RAM design and wrapping up mothballing the VMOS activity. It was during this period in about September of 1979 that one of the most important events that would play a major part in the future of TI occurred.

Roberto Fantechi , the design manager of the TI Bedford, MOS design department walked into Tony's shared Herman Miller Cube and said that he had an engineer in his office that Tony might be interested in talking to. The engineer turned out to be Dr. Surendar Magar who had a Phd in Signal processing and currently worked for Plessey Semiconductor where he was responsible for MOS design of Digital Signal Processors. Surendar was in the Bedford area

and had just decided to see if TI had any positions to suit his experience. Both Roberto and Tony interviewed Surendar and were extremely impressed with his experience and qualifications. Two days later Surendar found himself on a plane over to the US to be interviewed by John Hughes and Ed Caudel as a team member for the new S.P.C. program. Surendar was immediately offered a position on the design project. He was then suddenly faced with a tough decision to move from the UK to USA (far from the original thought of not having to move his home in Northampton to Bedford). He accepted the job due to a lifetime opportunity to work on a device that he thought could potentially commercialize DSP technology.

In November of 79 Ed Caudel traveled to TI Bedford to work with Surendar for two weeks on the specification and it was during this period that Surendar cleaned up some of Ed's ideas on the SPC architecture. In particular Surendar saw that the software approach to multiplication , also implemented on the i2920 and currently called for in the SPC architecture spec, would not fly for a DSP and he recommended changing to a 16X16 hardware multiplier with a 32 bit product. Also he recommended that the RAM size be increased to 144 words so that a 64 point FFT could be computed with 16 locations for temporary storage of coefficients. Later on significant other feature changes would be added that would set the scene for a device that would change the course of history for T.I.

The plan was for Surendar and his family to immediately leave for Houston and so his house was rented, the car sold and all family belongings were shipped to Houston. At the last minute, his departure was delayed due to complications with his wife's pregnancy and they had to stay in the UK for six months until his son, Gary, was born. TI arranged for temporary accommodation in UK, provided a car, etc., while they stayed in UK for this six months holding period. During this time Surendar worked on acquainting himself with TI's MOS design procedures, the current Architecture Specification of the S.P.C. as generated by Ed and completing the initial design of the multiplier.

The specification at that time also called for an on chip A-D converter. John Domogolla was the most experienced MOS device engineer working in MMP design and he was assigned to do the A-D converter. He also came over with Ed to liase with Surendar and Tony. The intent was for Surendar and Tony to start the US assignment in January of 1980 but Surendar's departure was delayed until March due to Surendar's wife's pregnancy complications.

Design Start for the S.P.C.

Tony reported into Jerry Rogers Office at 8600 Commerce Park on Monday 20th January 1980. Following on from the strategic decision to design the Alpha (TMS99000) chip in 2.5um SMOS Jerry assigned Tony the task of defining and characterizing the SMOS process and creating a comprehensive set of design guidelines for the design department for designing both Alpha and the SPC projects both of which were just about to start. The Alpha program under the design management of Richard Chang had a core team in place but the SPC had only Tony at this point in time and Surendar was still back in the UK. Ed Caudel was in the systems group refining the architecture spec and supported by technician Jerry Chandik.

Tony worked very closely with the MOS memory engineers on the 2147 SRAM project working with Cliff Rhodes and Jim Allen who was responsible for characterization work for SMOS in MOS memories. At that time the status of the process was very much in its infancy and a great deal of problems were being encountered with sub threshold conduction i n the 2.5um devices. This effect was modeled by a lowering of the threshold voltage as the drain voltage increased causing the device to conduct. For the dynamic techniques that were planned for the MOS design this was a serious design consideration since devices leaked charge away when the drain voltage exceeded 4.0V and SMOS was nominally a 5V process.

It was anticipated that the device would be produced in the MOS memory line fabricating the 2147 in LMOS (Lubbock MOS). Tony worked with Dobbie Walker in LMOS and negotiated a set of design rules in 2 weeks in order to meet the pressing need for Alpha and which had a full complement of approximately 60 rules total for the 8 mask process-a far cry from today's CMOS process that have about this many rules for each level.

Design Rules

Relying on the early production data from the 2147 some of the rules were backed off from the MOS memory requirements in order for improved yields at a small die size expense. Using these rules a test die was designed using effort from the Alpha project for complete characterization of the process with particular emphasis on the narrow width devices that would be used on the Alpha and SPC projects.

Ultimately this led to backing away from 2.5um as the channel length to 3.0um and defining an on chip generated Back Bias for both Alpha and the SPC in order to control the sub threshold leakage. One of the interesting parameters to emerge from this activity was the large increase in the body effect term for the narrow width transistors. An effect that had not been readily appreciated up to that time since all characterization data was being taken on 25um wide devices. This was the first MOS characterization exercise to include narrow width devices and led to a change in the Spice models being used to encompass the width changing parameters. The urgency of the Alpha project put great pressure on obtaining the correct Spice parameters and resulted in many late nights trying to correlate the data to make sense of the varying width parameters which was a phenomenon that was unknown at the time. Tony recalls having an Alpha program review scheduled for dissemination and reviewing the Spice models and at 3:00am He still had not managed to ascertain the gate width accurately from all the measurements in order to fix the Kp parameter of spice model. That review was scheduled for 8:00am of the same day. These initial design rules and Spice

models were released in approximately March of 1980. The design guidelines still needed to be formulated but also there was the project planning and manning for the SPC to be defined.

Program Manning.

Manning of any program at TI, as always, is one of the most difficult items to get under control. This is as true today as it was then. All programs were consistently undermanned. Surendar arrived in March and the only person available to support him on the design project was Tim Egging-a technician. Tim worked closely with Surendar at first doing sample cell layout to the new 3um SMOS design rules to support Surendar's logic/circuit design and concentrating on cell layouts for the 16X16 multiplier array. John Domogolla was working on the design of an A-D module as an independent project at the time. Although John completed the design of an A-D test die putting A-D on the main die was considered too risky with noise injection from the High Speed I/O and the substrate bias needed to control the leakage in the devices and John's work never got further than a Test Die.

Attempts to release people from other programs to staff the SPC failed. The other programs in the design area at that time were the TMS 99000 under Richard Chang, TMS 7000 under Kevin Mcdonough, the redesign of the TMS 9940 under Sergio Maggi, the TMS 1000 multi micro under Peter Koeppen and the Bubble memory controller under Joe Raymond. Alpha was the key program in the area required for DSG and was soaking up all available design effort and high level management attention.

In March of 1980 MMP started a massive hiring program to recruit college graduates and Tony was assigned by Jerry Rogers to coordinate this effort for the design department. It was during this time that Ed Caudel interviewed Wanda Gass (nee English) for a position in the systems group but quickly found out that Wanda was interested in silicon chip design. Although Wanda wanted to get into the field of medical electronics Ed thought that she might be persuaded to join Tony's SPC design program and introduced her to him. Tony recalls l the interview very well and his final comments on the interview form. Never had he interviewed a new graduate who knew so clearly what she wanted to do. Fortunately for TI Tony persuaded Wanda that whilst the SPC was not destined specifically for the medical market it could certainly find applications in that field and sold her on the program. Wanda was offered a position and became the 5th person on the program. Today Wanda is still with TI and is a TI Fellow for her contributions to DSP in TI.

It was during this hiring program that Joe Halphen was hired as a Layout designer and was assigned to work with Surendar who at this time was the Chief designer for the SPC with Tony being almost totally involved in the detailed characterization of the SMOS process and hiring program.

About this time Jerry Rogers was approached about using MMP design resources to design a custom DSP for IBM. Since Surendar was the only designer that had an in depth knowledge of Digital Signal Processing Jerry pressured both Tony and Surendar to reassign Surendar to this very important custom program. This was resisted by both Tony and Surendar and fortunately for TI they prevailed. This program was code named Yoda and was eventually set up in an enclosed area, known as the Yoda Fort, to protect the intellectual property rights of the customer, and led by Ken Davis.

Having persuaded Jerry to let Surendar stay on SPC program Surrendar worked on completing the logic design of the SPC. Joe Halphens first job was to do a complete logic diagram of the SPC before progressing on to chip layout. Joe pioneered using cell based Design Verification with a very significant schedule pay back. Prior to this Design Verification was done after a complete design which offered no learning curve and designs finished up with in excess of 50k errors. Design verification at this time was still left to the end of the program with the complete design being submitted for verification at the end of the design cycle. After one major task of correcting these errors it was still customary to generate one additional error for every two that were fixed.

There were two other key engineers assigned to the program during that first year. Tony had approached Richard Simpson in the Bedford design center to come and join the program. Richard was an expert MOS designer with a great deal of experience in MOS Logic having played a major role in the design and productization of the TMS 9914 GPIB chip which was one of the biggest runners in the 9900 family. Also Sam Rimawi from MOS memories had approached Tony about transferring into MMP. These two joined the program in the 3rd quarter of 1980. Since the SPC needed a ROM and RAM the timing of this was excellent. These designers represented the core team in the first year of the design program. Although the lack of manpower represented a slip to the schedule it had a serendipity in that Surendar had the opportunity to complete the first pass logic design and get a provisional chip plan completed before the final chip layout started in earnest. Wanda's first assignment was to complete FUSIM, the functional simulation program in use at the time. Joe Halphen completed the logic diagram and then moved on to generating cells with Tim Eggin. Richard Simpson commenced doing the Spice analysis of the ROM and Sam commenced the Spice work for the RAM which was a modified architecture of Tony's design used on the TMS9995..

Because of the hiring the design department had run out of space and the SPC team were moved out into a large empty office suite in the main Commerce Park location. The team was moved in with some old steel case furniture and a couple of filing cabinets and although it was not as plush as the Herman Miller furniture in the main office it had a very distinct advantage of open communication. The beauty of the environment was that all the people who were required to make a decision on the program were all located together. All the people were dedicated and felt that we were doing something new and exciting. They were all new and felt they

had to prove themselves. The program did not have a lot of high level management attention since the Alpha program was the key program in the organization and absorbed all the limelight.

In the September - October time frame of 1980 there were some major changes made to the organizational structure. Wally Rhines reassigned John Hughes to be the program manager for the Skywalker LAN (Local area network) program and asked Kevin Mcdonough to take over the program management of the SPC – a decision which would prove ultimately to have major ramifications to the overall success of the DSP program. At the same time the calculator design department, under K Bala was closed down, (an action that was a harbinger of difficult times ahead), and the people in it were incorporated into the MMP design organization. The majority of the people went into staffing the Yoda program with Ken Davis becoming the design manager for Yoda. The SPC picked up a senior chip designer Jess Andriesse and also a junior chip designer Bob Wagner. Jess took over the detailed chip plan activity and Bob was assigned cell layout. Roger Peters was a second time co-op student who was assigned to generate the logic simulation using ESIM.

Wayne Detloff was assigned by the 9900 product engineering group to work with the SPC design team. Wayne started work at the end of 1980 with his responsibility to write the test program for the SPC.

Early in 1981 the Alpha program taped out and with the tape out it freed up more chip layout people. Grace Robertson joined the program as a chip layout designer and also Sandy Tran who had been hired in the same recruitment campaign as Joe Halphen the previous year. From a management perspective the program could not have been better. With the Alpha program taping out it relieved a lot of the backlog in Design services for editing the cell layouts and more importantly, skilled people to man the program.

Starting into 1981 the program, from a design management perspective, was ideally staffed and everything was progressing well. No other subsequent program that Tony worked on was ever so fortunate as to have such a well balanced and dedicated design team that worked so well together. The "Esprit de corps" was fantastic and in Surendar's words written some 20 years later, " We believed enough to work hard and had a feeling that we were on to something big".

The goal had been set to present the SPC at the International Solid State Circuits Conference in February of 1982 and for this to happen the paper had to be complete with a chip photograph in October of 81. In January of 81 this goal looked attainable and everyone was committed to it.

Microcomputer vs Microprocessor SPC

In January of 1981 Kevin Mcdonough brought his experience to bear to make some important changes to the current specification of the SPC program. Up to this time the spec for the SPC call for a microcomputer architecture packaged in a 24 pin DIL package. With Kevin's experience with the TMS 7000 he realized that this was a major mistake and advocated a microprocessor architecture and bringing the memory bus out. This increased the pin count to 40. Also at the same time Gary Swoboda (now a TI Fellow) worked with the design team to include necessary features to make the chip self emulating. This included adding an extra level of stack amongst other things the major task already being accomplished by creating access to the memory bus.

Fortunately these changes were not too drastic to the design program. Surendar reworked the logic in January of 1981, since some of the instructions had become two cycle instructions.

Bad Economic News

In February of 81 the bad business environment caught up with the SPC program and unfortunately Sam Rimawi was part of the reduction in force having just completed the initial Spice analysis of the RAM. This was a complete surprise to everyone on the program since no rumors had reached the SPC team of any impending layoff.

TI these days is a much more humanitarian organization than it was back then. Thankfully a legacy of the late Jerry Junkins. In J Fred Bucy's days the supervisors were informed of the people who were to be let go. The employee was escorted by the supervisor to the department managers office where he was informed he no longer had a job and to complete the paper work. He was then escorted back to his desk where he was allowed to pack his personal possessions. The supervisor took his badge and he was escorted off the premises. Tony had the unenviable task of informing Sam. He recalls being told to report to Jerry Rogers office on arrival at work where he was informed that Sam was being let go. When he started to protest Jerry said "There's nothing you can do about it - it's a done deal", and it was, except that Tony allowed Sam to keep his badge for the day so that he could see if his memory colleagues could find him a job. Unfortunately all departments are in the same boat in such economic times so unfortunately Sam left at the end of the day but with a little more dignity than the majority. To day these events are handled in much a more humanitarian manner with advance notice of layoffs and options that the affected employees can exercise. This event was entirely unexpected by all on the SPC and took the whole team by surprise and they were very sad to see Sam go.

Since only the preliminary Spice work had been completed Jim Tiller joined the program to complete the checkout of the ram using updated layout paracitics.

Design Methodology

Back in the early 80's the design methodology jargon for chip layout was Strip line architecture vs Island layout. The modern name for strip line layout today is data path. The Island approach was to keep each logic block separate and couple it with metal lines. This was very wasteful of chip

area particularly since the devices only had one metal level. The strip line architecture was to structure the data paths as they are in today's methodology and have the individual cells integrated on a fixed pitch data path. Back in the 80's when all cell layout was done by hand this had a major effect on the layout time particularly for a structured data path like a DSP. Management and design team had a pleasant surprise when comparing transistor layout productivity achieved on the SPC to that of the Alpha chip. The productivity was mainly due to the simple architecture and the repeated cell structure. The SPC chip layout was basically composed of 4 blocks being the data path (Strip line architecture) Ram, Rom and program control.(See fig 1)

Design Verification

Two forms of Design verification were used. As already mentioned Joe Halphen pioneered the cell based DV, which significantly reduced design rule violations. At that time TI's Automation department (DAD) had just released the Schematic Verification program. Wanda Gass took the responsibility of adding all the signal names on the layout data base and running the SV program utilizing a prototype designer terminal that was designed by DAD. Wanda spent 3 months pioneering schematic verification on the SPC.

The SPC was one of the first programs to use Schematic verification. Since it was new the designers did not trust it and an independent audit of the layout was conducted by two other engineers locating all the transistors on the design and making sure they were connected correctly. It took Perry Lou and Aman Khosrovi two weeks to complete the activity. Whilst they found no transistor hook up errors they did find some non ideal clock line distribution and power and ground routing . which needed correcting.

At the time the SPC was the largest chip to be released from the MMP design department with the largest RAM with a total chip count of 33000 transistors. With today's automated technology this would be one small module on a complete die and designed by one person using automated tools. Twenty five years ago all cells were drawn by hand on a mylar grid and then had to be digitized for entering into the data base for editing on the TILES interactive graphic system. Due to limited resources time had to be booked on these terminals by the chip designers so shift work was the order the day. Spice and ESIM had to be run on the IBM mainframe and this meant walking over to the main design office in the building at 8601 commerce park to enter the data sets on the 990 terminals and collect the line printer outputs for run analyses.

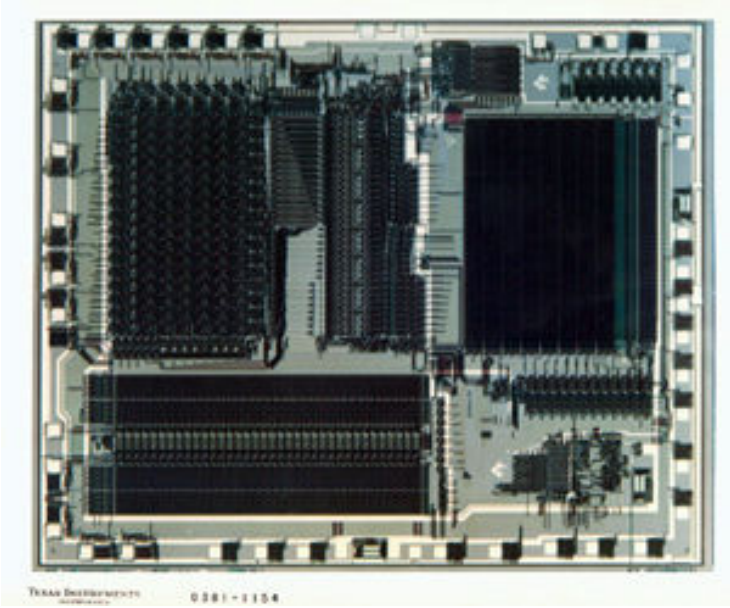

Fig 1. The TMS 32010. The device that changed the destiny of a corporate giant.

Device Name

The very first name conjured up for the SPC by the design group was to call it the TMS10000 series. The 10000 coming from the TMS 1000 which was also a Harvard architecture and 5 digits were necessary to convey measure of performance of the 5Mhz clock speed (Back then it was fast) and following on from the TMS 99000 scenario. Wayne Detloff recalls that the layout team had already encoded the name on the die in metal as TMS 10010 since the tape out date was imminent. Kevin Mcdonough did not like the 10000 and undertook to form a minor committee with MMP marketing to come up with the name. Wayne recalls that it was probably fortunate that Kevin did change the name since 10010 was apparently CB radio jargon to obey the call of nature.

Since the device had a 32 bit ALU (Arithmetic Logic Unit) it was decided to incorporate this feature in the name with 01 being the first device and an extra Zero added on to convey the performance aspect. Hence the name TMS 32010 was born and just in time to make it onto the die before it went for tape out

Tape Out

TI referred to tape out as PG release after the old style Pattern Generators used for generating the Masks. PG release occurred in September of 1981. Despite all the checking the software for the ROM programming had eliminated the cell that would have placed the ROM Program. Unknown to any of the design team at the time if a cell was placed with no geometry's in it the PG program deleted that cell. Therefore the ROM code did not have a cell for it to be placed into so the computer program ignored the ROM Code. Since the time was running out for getting a chip photograph for the ISSCC article deadline and the ROM was diffusion coded it was the first mask in the process it was decided to proceed without the ROM code since the device could be tested without it and it would be corrected on the second pass. Observation of the photograph published in the 1982 ISSCC proceedings will show the lack of programming in the ROM.

Processing

The Dallas MOS 2 wafer Fab was to do the processing. The masks were shipped up and the ISSCC schedule allowed 3 weeks for processing. Two lots were started with the first being a hot lot. Processing went according to schedule until about two thirds through the cycle when the process engineer called Tony and said that a processing step had been done wrong and the lot would zero yield and what did he want them to do. The other lot would not make it in time for a chip photograph so Tony asked the engineer to complete the lot only showing the visible levels. This was agreed and the devices were completed missing some of the steps in the process. It was learnt about 3 months later that this had contaminated the line and it had to be purged. Processing was as much in its infancy back in those days as design. It is difficult to see how such a catastrophic error would be made today. Anyway the wafers were shipped to Commerce Park. Unfortunately there was a problem with the camera equipment in Houston and Richard Simpson had to drive to a commercial photographic studio that had the necessary equipment to be able to photograph the wafer for the chip photograph for the ISSCC paper. The photograph was not excellent but did show the structure of the device. The paper was put in the mail the same day with just two days left before the ISSCC deadline and it is this photograph that appeared in the ISSCC 82 journal.

The backup lot arrived about a week later and went straight to the tester where Wayne Dettloff and Richard Simpson proceeded to check the circuit out.

The results exceeded all expectations with the device being fully functional on the first pass. The SPC team were in effect following Alpha on stage . Alpha had first silicon approximately 4 months before and also had a similar success and the first circuit had booted up all the 990 software from the first pass silicon.

Jerry Rogers had bet Jim Huffines (the MMP marketing manager) a crate of wild turkey whisky that Alpha would work on the first pass. Jim thought he was on to a pretty safe bet since such a thing had not happened before. The presentation was made in the cinema complex across the street from Commerce Park during one of Wally Rhines MMP division meetings.

With such a success the design team were extremely happy but after the initial euphoria there was the task getting the device to a production ready state. With a completely new process there were a lot of teething troubles to overcome. Tony recalls that two of the major problems were the fact that during the design phase fringe capacitance had not been accounted for. Whilst some devices would work at the design goal there was not enough margin to go into production. Wayne and Richard worked through a number of speed path enhancements during the next months but a 90% shrink was needed in order to meet spec. The other major difficulty first isolated by Bill Cordan on the Alpha program and subsequently found to be an even bigger problem on the SPC was inductive bump on the VSS line as the 16 bit I/O switched. This caused the whole ground plane to pulse when the I/O's discharged exceeding the TTL zero level. Since only one pin was available for VSS this led to some innovative ground bussing techniques to meet the TTL low level requirement. The design team were extremely thankful that they had not tried to implement the A-D on to the SPC.

ISSCC Presentation.

The SPC was presented at the 1982 ISSCC conference in February by Surendar Magar. Surendar did an excellent job of presenting it. Contrary to most presenters Surendar appeared to be in his element. He was very professional, strutting around the stage as though he owned it in complete confidence, pointing at the foils with the light pen and articulating the major points of the architecture. In the panel session in the evening all the questions were centered on the 32010 with John Hughes being the TI panelist and fielding the questions.

Publications

An article on the 32010 was published in the February 24th 1982 issue of Electronics and entitled "Microcomputer with 32-bit arithmetic does high-precision number crunching", by authors K.Mcdonough, E. Caudel, S.Magar and A. Leigh. The device was awarded the product of the year award from Electronics Magazine in 1982.

Epilogue

Today the whole 39000 people at TI are supported by DSP and Analog. The majority I am sure do not know the origins of their jobs or what led up to TI being in its current position. To be sure the position that TI finds itself in today is as the result of excellent business decisions and execution from those people who stepped into the management positions as the device was turned into a business. First was John Hayn followed by Dave French , John Scharisbrick and Mike Hames over the next 18 years. But in the early days serendipity and luck also played a major part in shaping the destiny of TI in the new millennium. From Harveys Cragons proposal, Intels disclosure of the i2920, Ed Caudel's interest in generating the first architecture spec, Surendar Magar with his Phd in Signal processing and turning up on TI's doorstep at just the right time to refine the spec, Jerry Rogers acquiescence on Yoda, Kevin Mcdonough's memory expansion, Gary Swoboda's self emulation, and the team meeting the ISSCC deadline. These are the major items contributing to the success of the 32010 and laid the first stepping stone for others to build on.

It is interesting to note that the NMOS 32010 did not have a very long life. Whilst it was going into qualification for production in 1983 a second source agreement was agreed with General Instruments. In exchange for second sourcing the 32010 GI was contracted to do a CMOS version called the 320C10 that was compatible with TI's new CMOS

process. The CMOS version took over from the NMOS version and the core CPU of this CMOS device became the heart of a range of 320 devices continuing into the 90s.

A few of the original team members made their long term careers with TI, others have gone on to develop new careers and still others have retired. Sadly Ed Caudel passed away from cancer in 1984 and was not destined to see how his efforts would effect the destiny of TI and the changes that TI's DSP's would make to the world. As Tony wrote in his retirement message in 1998, "To all my friends and colleagues all over the world I consider myself privileged to have worked with you all. Together we have made a difference. The world is recognizably a different place as a result of our DSP efforts". In Surendar's words in reply . "As co-founders of the TMS 32010 DSP group, many of us worked in a closely knit team, in a warehouse like building, with one desire - produce a commercially successful DSP chip. We were fortunate enough to realize the dream with a combination of technical innovation of team members, TI management support and TI's technology prowess. Most engineers start out with such a dream but only a few are lucky enough to get an ideal opportunity to realize it. Well, we were lucky . We believed enough to work hard and had a feeling that we were on to something big. But yes, we never could have imagined that our pioneering DSP work will one day change the course of entire TI".

Poetic words that need to be recorded in TI History.

People that worked with Tony will recall that he was often want to adapt some of Winston Churchill's famous quotations to fit particular situations in the design review process. For the importance of the TMS32010 to TI's history it seems fitting to adapt Churchill's most famous quotation to end this narrative. "Never, in the field of [TI IC design], was so much owed by so many to so few". This is not meant to downplay the importance of the decisions and actions made by others who came after and who turned the chip design into a major and very successful business opportunity for TI but, never-the-less, without the exemplary execution by the initial team in building the first stepping stone in the DSP road map the TMS 32010 history and the subsequent course of TI would need to be rewritten.

Author's note.

The views and recollection of events as outlined in this article are my recollection of events as viewed from my position as Design Manager for the 32010 design program. I have tried to be as factual as possible in recounting these events and but I was not privileged to have first hand knowledge of the events leading up to the formation of the program and would like to acknowledge the help received from Wally Rhines, and John Hughes in recounting those aspects of the program. In addition I do not have access to any of the TI archived materials and the material and dates are purely from memory. Views expressed are entirely my own and I accept that others may hold different opinions. I would be pleased to receive any correspondence on this article –in particular from any of the people whose names are mentioned and with whom I have lost contact.

Some reflections on the future.

The effects of global communication in the destabilization of society.

It is 25 years since TI launched its Digital Signal Processing initiative and around 15 years since the technology became a world wide media communication tool. As I wrote in my retirement message to Tiers "The world is recognizably a different place as a result of our DSP efforts".

All inventions have positive and negative effects on society. The invention of gunpowder by the Chinese for entertainment resulted in its use for weapons of war. The automobile as a replacement for the horse and carriage opening up frontiers of travel to society but at the expense of pollution and increasing global warming. The invention of nuclear power resulted in society being terrorized by its use as a weapon instead of its peaceful use of power generation.

Digital Signal Processing opened up the world to global communication by any individual with a computer and knowledge of the world wide web. I question whether nature intended that every one should know what was happening in the world at the same instance in time and what the overall impact to society is as a result. Is the growth of terrorism a result of global communication spreading the idea or is it a benign information transfer medium? Are we playing to terrorist agenda by reporting the terrorist demands and distributing their atrocities in such graphic detail to the rest of society thus inciting religious and ethnic confrontations?

If enough heat is applied to water in a vessel the normal stable equilibrium is turned into unstable boiling cauldron. Are we unconsciously, through the media, exciting society into an unstable situation?

As an engineer I make the analogy of society being a closed loop feedback system. Feedback can be either positive or negative. Positive feedback results in an unstable situation and negative feedback results in a stable situation. If the gain of a system is increased too high it will result in instability. I suggest that we are at that point in society where the gain of the system has been increased to provide instant feedback via the media that the situation is in danger of self perpetuation and we are on the verge of a breakdown in ethnic and religious social values. There have been many instances in the past where it has been demonstrated that mass media reporting of a societal behavior has caused an increase in that type of behavior in subsequent instances just because the news media reported the behavior. This then poses the question does the news media report the news or create it?

A classic solution to the engineering problem of stabilizing a feedback system is to decrease the gain or reduce positive feedback. In the social sense this would mean delaying (or eliminating) the reporting of the events so

that response time between cause and effect is increased. This has been done in past wars. However a major problem that American society would have with this is the right of free speech. The news media would not accept this despite any adverse consequences of their reporting and would view it as censorship.

Whether the engineering model could be adapted for modeling social behavior I do not know but I believe the world needs to understand the implication of instant global mass media information feedback on the stability criterion of society.

I am reminded of the theme of the 50's film "The Forbidden Planet" where the inhabitants developed a machine that enabled them to conjure up physical powers from their thought processes. It would give them a better life by reducing manual work. Unfortunately the physical powers were not confined to their conscious thoughts but were enabled by subconscious thoughts as well. Any person that offended another was eliminated by some mysterious force that they did not understand. Since there was no evidence of what had happened the rest went in fear of the others. .Fears within the society, directed by suspicions of fellow members, led to an uncontrolled release of energy that eventually killed all except one, a father and his daughter and they survived since they harbored no ill thoughts to one another. The society never understood what it was that was killing them and could not combat the terror amongst them.

I am not suggesting that the Internet is in any shape or form equivalent to the machine in the example quoted. The moral of the story is that we as a society need to understand the negative aspects of our inventions. It is easy to design something to do what you want it to do. It is much more difficult to design something not to do what you don't want it to do. We have designed a system to enable the information highway. For the most part it has made major benefits to society but do we really understand if there are any "subconscious" aspects that we need to investigate to ensure a safer tomorrow and, if so, how do we apply them?

I would propose that Texas Instruments, being the leader in Digital Signal Processing, should take the lead and provide a grant for a social science university program to come up with a model that can be used for predicting the consequences of mass media information on the stability criterion of society. Maybe there is such a program currently being worked on at some university that I do not know about. If anyone has any information I would be pleased to receive any communication on this topic or indeed on any of the topics in this article. I can be reached by e-mail at awleigh@earthlink.net.

Anthony (Tony) Leigh

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About the Author

Anthony (Tony) W. Leigh C. Eng., MIET., PE.(Inactive)

Tony was born in Wimborne in the county of Dorset, England in 1938. He graduated from Queen Elizabeth's Grammar School, Wimborne in 1954 and was accepted into the deHavilland Aeronautical Technical School where he completed an electrical engineering apprenticeship and obtained a Higher National Certificate in Electrical engineering in 1961. Upon completion of his apprenticeship he gained employment in the Sea Vixen Design Office of the deHavilland Aircraft Company in Hatfield, England where he was responsible for the electrical installation of the Red Top missile into the Sea Vixen Aircraft. In 1963 he transferred into the Flight Simulation Department where he developed a hybrid Analog-Digital computer system to provide a visual display of a simulated airfield to aid pilots in developing the Autoland system of the Trident Airliner.

He left in 1967 and was employed by Television Audience Measurement to design a digital computer utilizing Fairchild RTL, specifically for processing punched card TAM data and converting it to 7 track magnetic tape ASCII format to produce a weekly report of TV viewing habits in the UK.

He joined the Equipment and Components division of Texas Instruments, Bedford, England in 1969, as a project engineer, completing several custom projects before moving into the MOS Design department where he completed the design of two time of day clock chips in PMOS technology and an I2L logic chip for the TIFAX system - the first commercial application for receiving the BBC's CEEFAX on British television.

In 1976 he transferred to the Memory Design Department of TI based in Stafford, Texas where he was responsible for the design of TI's 4K NMOS SRAM Program. He returned to England in 1978 where he completed the design of a VMOS memory mapper and the RAM design on the NMOS

TMS9995. In 1979 Jerry Rogers asked Tony to go back to the US as the Design Manager for the 3um SMOS Signal Processing Computer which became known as the TMS32010 and was TI's very successful entry into the commercial DSP market. Tony also led the design of the next generation of DSP devices, the TMS 32020 and the 1um CMOS TMS 320C30. In 1992 he wrote the design rules and completed the memory designs for the TMS 320C50 and TMS320C51 devices of the Mosaic program which led TI's entry into the cellular telephone market. In 1994 he headed up the CMOS Design Council whilst moving into the area of Quality Assurance, writing and promoting the TI World Wide design guidelines for "Design in Reliability".

Tony Retired in October 1998, after a very satisfying engineering career, and with 29 years of TI service.

Tony is married and currently lives in Richmond, Texas with his wife Susan. He has 5 children and three grandchildren. His interests are designing building and flying radio controlled model aircraft, collecting vintage model aircraft engines, painting and woodworking .